Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (Currently Amended) The method of claim ~~1~~6, asserting a first valid data field of said first entry of said reorder buffer after said execution of said first instruction but before said determining whether said first register value should be copied from said first alias register to said first real register, said asserted first valid data field indicates that said first register value is valid for copying from said first alias register to said first real register.

3. (Original) The method of claim 2, further comprising reading said first valid data field in determining whether said first register value should be copied from said first alias register to said first real register.

4. (Original) The method of claim 3, further comprising copying said first register value from said first alias register to said first real register if said first valid data field indicates that said first register value is valid for copying into said first real register.

5. (Original) The method of claim 2, further comprising deasserting a second valid data field of a second entry of said reorder buffer, said second entry including a second alias register previously associated with said first real register, said deasserted second valid data field indicates 4 that said second register value is not valid for copying from said second alias register to said first 5 real register.

6. (Currently Amended) ~~The~~ A method ~~of claim 1, further~~ comprising:

providing a reorder buffer comprising a plurality of entries associated respectively with a plurality of instructions;

executing a first instruction of said plurality of instructions which generates a first register value for a first real register, said first register value being stored in a first alias register identified in a first entry of said reorder buffer associate with said first instruction;

determining whether said first register value should be copied from said first alias register to said first real register approximately at a time when first entry of said reorder buffer is needed for a second instruction that is younger in order than said first instruction;

providing a data commitment table comprising a plurality of entries associated respectively with a plurality of real registers including a first entry associated with said first real register, said first entry of said data commitment table comprising a committed data location field to indicate if a second register value generated by a third instruction is stored in a second alias register or in said first real register, and a reorder buffer index field to identify a second entry of said reorder buffer containing said ,second alias register if said second register value is stored in said second alias register;

determining whether said second register value is in said second alias register or in said first real register by reading said committed data location field of said data commitment table;

deasserting a second valid data field of said second entry of said reorder buffer if it is determined that said second register value is in said second alias register~~, said deasserted~~to ~~indicates~~ indicate that said second register value is not valid for copying from said second alias register to said first real register; and

writing an identifier for said first entry of said reorder buffer in said reorder buffer index field of said first entry of said data commitment table.

7. (Currently Amended) ~~A~~ The processor system ~~comprising~~of claim 12, wherein~~:~~

~~a reorder buffer comprising a plurality of entries associated respectively with a plurality of instructions;~~

~~an execution unit to execute a first instruction of said plurality of instructions which generates a first register value for a first real register, said execution causing said first register value to be stored in a first alias register identified in a first entry of said reorder buffer associated with said first instruction; and~~

~~an allocator to add new instructions into said reorder buffer.~~ said allocator determining whether said first register value should be copied from said first alias register to said first real register approximately at a time when said allocator determines that said first entry of said reorder buffer is needed for a second instruction that is younger in order than said first instruction.

8. (Currently Amended) The processor system of claim ~~7~~12, ~~further comprising a~~ wherein said retirement unit to assert a 2 first valid data field of said first entry of said reorder buffer after said execution unit has executed 3 said first instruction but before said allocator determines whether said first register value should be copied from said first alias register to said first real register, said asserted first valid data field 5 indicates that said first register value is valid for copying from said first alias register to said first 6 real register.

9. (Original) The processor system of claim 8, wherein said allocator reads said first valid data field in determining whether said first register value should be copied from said first alias register to said first real register.

10. (Original) The processor system of claim 9, wherein said allocator causes a copying of said first register value from said first alias register to said first real register if said first valid data field indicates that said first register value is valid for copying into said first real register.

11. (Original) The processor system of claim 8, wherein said retirement unit causes a deasserting of a second valid data field of a second entry of said reorder buffer, said second entry identifying a second alias register previously associated with said first real register, said deasserted second valid data field indicates that said second register value is not valid for copying from said second alias register to said first real register.

12. (Currently Amended) ~~The~~ A processor system ~~of claim 7, further~~ comprising:

a reorder buffer comprising a plurality of entries associated respectively with a plurality of instructions;

an execution unit to execute a first instruction of said plurality of instructions which generates a first register value for a first real register, said execution causing said first register value to be stored in a first alias register identified in a first entry of said reorder buffer associate with first instruction;

an allocator to add new instructions into said reorder buffer;

a data commitment table comprising a plurality of entries associated respectively with a plurality of real registers including a first entry associated with said first real register, said first entry of said data commitment table comprising a first committed data location field to indicate if a second register value generated by a third instruction is stored in a second alias register associated with said first real register or in said first real register, and a reorder buffer index field to identify a second entry of said reorder buffer identifying said second alias register if said second register value is stored in said second alias register;

~~wherein said~~a retirement unit to determines whether said second register value is in said second alias register or in said first real register by reading said first committed data field of said data commitment table;, ~~wherein said retirement unit~~to causes a deasserting of a second valid data field of said second entry of said reorder buffer if said retirement unit determines that said second register value is in said second alias register, said deasserted indicates that said second register value is not valid for copying from said second alias register to said first real register;, and ~~and wherein said retirement unit~~to causes a writing of an identifier for said first entry of said reorder buffer in said buffer index field of said first entry of said data commitment table.

13. (Canceled)

14. (Currently Amended) The computer readable medium of claim ~~13~~18, wherein said one or more software modules to further assert a first valid data field of said first entry of said reorder buffer after said execution of said first instruction but before said determining whether said first register value should be copied from said first alias register to said first real register, said asserted first valid data field indicates that said first register value is valid for copying from said first alias register to said first real register.

15. (Original) The computer readable medium of claim 14, wherein said one or more software modules to further cause a reading of said first valid data field in determining whether said first register value should be copied from said first alias register to said first real register.

16. (Original) The computer readable medium of claim 15, wherein said one or more software modules to further cause a copying of said first register value from said first alias register to said first real register if said first valid data field indicates that said first register value is valid for copying into said first real register.

17. (Original) The computer readable medium of claim 14, wherein said one or more software modules to further cause a deasserting of a second valid data field of a second entry of said reorder buffer, said second entry including a second alias register previously associated with said first real register, said deasserted second valid data field indicates that said second register value 5 is not valid for copying from said second alias register to said first real register.

18. (Currently Amended) ~~The~~ A computer readable medium adapted for execution by a processor comprising ~~of claim 13, wherein said~~ one or more software modules to ~~further~~:

generate a reorder buffer containing a plurality of entries associated respectively with a plurality of instructions;

execute a first instruction of said plurality of instructions which generates a first register value for a fist real register, said first register value being stored in a first alias register identified in a first entry of said reorder buffer associated with said first instructions;

determine whether said first register value should be copied from said first alias register to said first real register approximately at a time when said first entry of said reorder buffer is needed for a second instruction that is younger in order than said first instruction;

provide a data commitment table comprising a plurality of entries associated respectively with a plurality of real registers including a first entry associated with said first real register, said first entry of said data commitment table comprising a committed data location field to indicate if a second register value generated by a third instruction is stored in a second alias register or in said real register, and a reorder buffer index field to identify a second entry of said reorder buffer

containing said second alias register if said second register value is stored in said second alias register;

determine whether said second register value is in said second alias register or in said first real register by reading said committed data location field of said data commitment table;

deassert a second valid data field of said second entry of said reorder buffer if it is determined that said second register value is in said second alias register, said deasserted indicates that said second register value is not valid for copying from said second alias register to said first real register; and

write an identifier for said first entry of said reorder buffer in said reorder buffer index field of said first entry of said data commitment table.

19-30. (Canceled)